CommAgility

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5GNR Project

Overview

- Commagility 5GNR Internal Project Overview
  - Objectives
- Possible support activities

- Multi-access Edge Computing (MEC) trends
- gNB Architecture Proposal
  - MPSoC+FPGA
  - Moderate throughput & BW
- Extended Architecture for High Throughput & BW

- PHY software architecture
  - PHY software/hardware partitioning
  - Acceleration Model
  - Planned accelerators

- CA Design & Testing approach
- Reference C chain

Project Objectives

- Commagility has been 10 years at the forefront of LTE system development and aims to be so for 5G
- Extending Commagilty Products and Know-How on 4G with those for 5GNR
  - 5GNR IP for gNB and UE
    - 5G Reference Chain (ANSI C, fixed point)
    - 5G software and firmware IP for real-time implementation
    - Real-time implementation on validation platform, MPSoC + Ultrascale^{+} FPGA
  - 5GNR boards

Project Objectives

- 5G gNB Reference Chain
  - Blueprint for real-time algorithm development for a implementation on a product platform
  - gNB physical layer software
  - Tested for 3GPP performance
  - Validated against Keysight T&M and test vectors
  - Protocol stack software for Linux PC

- 5G real-time integrated system implementation & software and firmware IP
  - Blueprint for microarchitectural design of the product platform
  - Integrated system on validation platform, e.g.MPSoC + Xilinx Ultrascale^{+} FPGA (or Versal)
  - 5G IP for end-to-end system:
    - LDPC, Polar, Channel Estimator, Equalizer, Modulation chain, Demodulation chain, RX and TX HARQ Control, Channel Multiplexer, Channel Demultiplexer, Pre-coding, Digital Beamforming, PRACH, Sounder, Measurements, PUCCH, OFDM signal generation, OFDM signal receiver

Project Objectives

- 5GNR Boards
  - Boards design for ODM
  - Board level solution for private networks
  - Board level solution for end-to-end test systems
  - Inclusion of integrated RF solution for end-to-end system funtionality

- 5G UE Reference Chain, RT integration system implement, and SW&FW IP
  - Reference system for test vector generation
  - Integrated real-time system implementation for end-to-end gNB testing

5GNR Development steps

- C reference implementation
- Micro architecture design
  - Processor architecture
  - Memory architecture
  - Interconnect architecture
    - Resource allocation
- System architecture design
  - Coarse grain task partitioning
  - HW/SW partitioning
  - Micro-architecture components binding
- Signal processing blocks for computationally intensive data processing algorithms
- System control design
  - Control
  - Data flow
- System integration

5GNR Development Support

- PHY System design implementation
  - Northbound interface setup
  - Southbound interface setup
  - Support for HW component development (in the case of Soc or FPGA product platform)
  - Peripherals (i.e. hardware accelerator) drivers
  - Interconnect development
  - Control (system, sub-system, component) software development
  - Signal processing software components development
  - System integration & testing
- Digital RF FE development support
  - Southbound interface setup
  - Interconnect development
  - BB FE control & signal processing software development
  - RF control (handles) software development
  - System integration & testing
- Testing support
  - End-to-end system integration & testing
  - 3GPP Conformance testing
  - Deployment of Commagility 5GNR UE
  - Phased testing approach including early stage testing capabilities