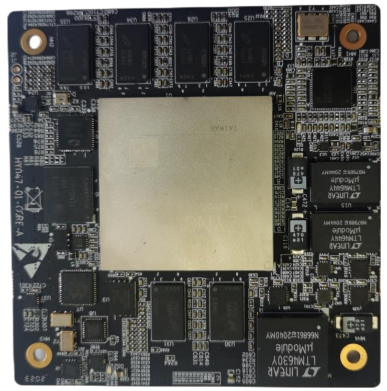
RISN-5088 高速多通道数据/射频采集卡



北京启扬日升科技有限公司

Roadmap to Meet Current and Future Market Needs

Performance

ZYNQ RFSoC

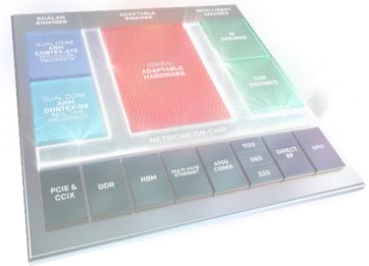
GEN 1

4GHz
of Analog Bandwidth

GEN 2

5GHz
of Analog Bandwidth

6GHz
of Analog Bandwidth



XILINX VERSAL™

Current Market Needs

Smaller, Low-Cost ⇔ More Compute per ADC/DAC

- ✓ More integration
- ✓ Lower digital power per channel
- ✓ More processing per channel
- ✓ Lower price point
- ✓ Greater Instantaneous Bandwidth and more carriers

2018 | 2019 | 2020 | 2021 | 2022+

XILINX

Scalability Across the Portfolio

			ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
		Radio	●	●	●	●	●	●	●	●	●	●	●	●
		Backhaul				●								
		Baseband	●											
		Fixed Wireless Access				●	●	●	●			●		●
		Cable R-PHY				●							●	
		Satellite / Test & Measurement			●		●		●	●		●		●
		Radar / SIGINT					●		●	●	●			●
Analog Signal Chain	RF Data Converter Subsystem	RF-ADC w/DDC # of ADCs	-	8	8	8	16	16	8	2 4	8	4 8	8	16
		RF-ADC w/DDC Max ADC rate (GSPS)	-	4.096	4.096	4.096	2.058	2.220	2.5	5.0 5.0	2.5	5.0 5.0	5.0	2.5
		RF-ADC w/DDC Resolution (bits)	-	12	12	12	12	12	14	14	14	14 14	14	14
		RF-DAC w/DUC # of DACs	-	8	8	8	16	16	8	4	12	8	8	16
		RF-DAC w/DUC Max DAC Rate (GSPS)	-	6.554	6.554	6.554	6.554	6.554	10.0	10.0	10.0	10.0	10.0	10.0
		RF-DAC w/DUC Resolution (bits)	-	14	14	14	14	14	14	14	14	14	14	14
		SD-FEC	8	-	-	8	-	-	-	-	8	-	8	-
		Real Multi-band support per ADC	-	1	1	1	1	1	1	2	1	1	1	1
		RF input Freq max. GHz			4			5				6		
		Decimation / Interpolation			1x, 2x, 4x, 8x			1x, 2x, 4x, 8x		1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x			20x, 24x, 40x	
Programmable Logic (PL)	Integrated IP	System Logic Cells (K)	930	678	930	930	930	930	488	930	930	930	930	930
		DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1872	4,272	4,272	4,272	4,272	4,272
		GTY Transceivers	16	8	16	16	16	16	8	16	16	16	16	16
		PCIe® Gen 3x16, * and Gen 4x8	2	1	2	2	2	2	-	2*	2*	2*	2*	2*
		100G Ethernet w/RS-FEC	2	1	2	2	2	2	1	2	2	2	2	2
Package Footprint	D1156	35x35	■											
	E1156	35x35		■	■	■			■	■		■	■	
	G1517	40x40		■	■	■				■		■	■	
	F1760	42.5x42.5					■	■						■
	H1760	42.5x42.5									■			

Package Migration

Package Compatible

XILINX.

Introducing Zynq UltraScale+™ RFSoC Gen 3

Extended RF performance for more use cases

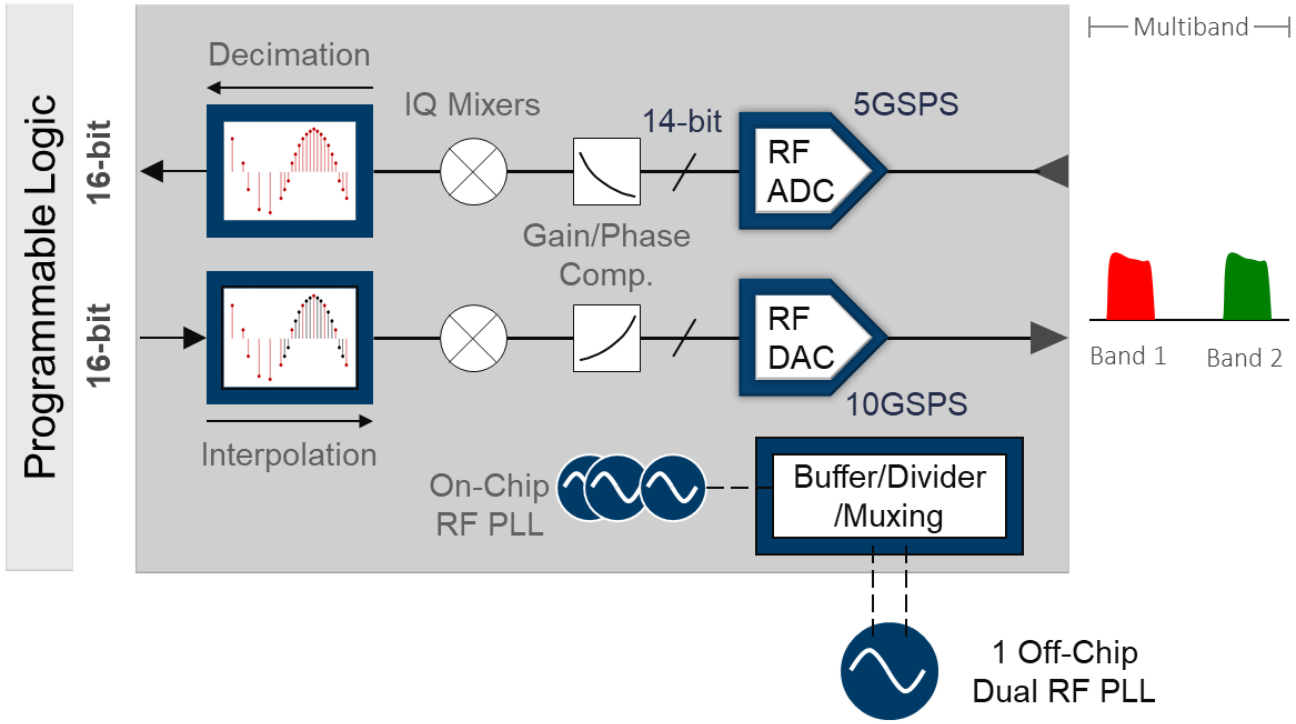
- Full Sub-6GHz Direct-RF support
- 8 ADCs up to 5GSPS or 16 ADCs up to 2.5GSPS
- Up to 16 DACs up to 10 GSPS
- 14 bit performance
- Extended mmWave interfacing

Reduced BOM and system cost

- Enhanced clocking distribution simplifies PCB board design
- Eliminates onboard clocking component cost

Simplified design and greater flexibility

- Full multiband, multi-standard support
- Additional interpolation and decimation off loads Programmable Logic
  - (1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x)



XILINX.

RFSoC PCIe 卡

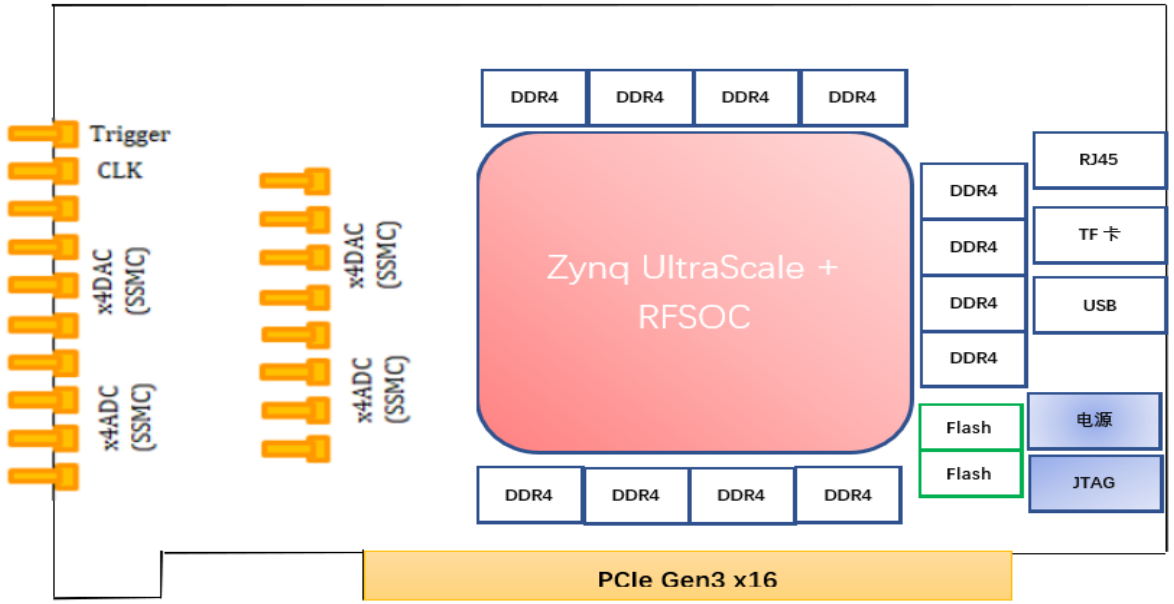
- 基于Zynq RFSoC三代 FPGA
- 8路最高5G SPS ADC
- 8路最高10G SPS的DAC
- 标准PCIe全高半长板型（167 x 111 mm ）
- PCIe Gen3 x16，高速数据通讯
- PL部分8GB DDR4
- PS部分4GB DDR4
- 支持外部时钟输入
- 1000Base-T以太网（RJ45）端口（CPU端）
- USB接口支持

RFSoC PCIe 卡的前端子卡

可以选择多种射频前端子卡，以适应不同输入

选项编号	频率范围	ADC/DAC
1	10M-3GHz	8ADC 通道
2	700M-1600MHz	8ADC 通道
3	DC-COUPLED_6552	8ADC 通道，LMH6552 运算放大器
4	DC-COUPLED_5567	8ADC 通道，LMH5567 运算放大器
5	700M-1600MHz	4ADC 通道 4DAC 通道

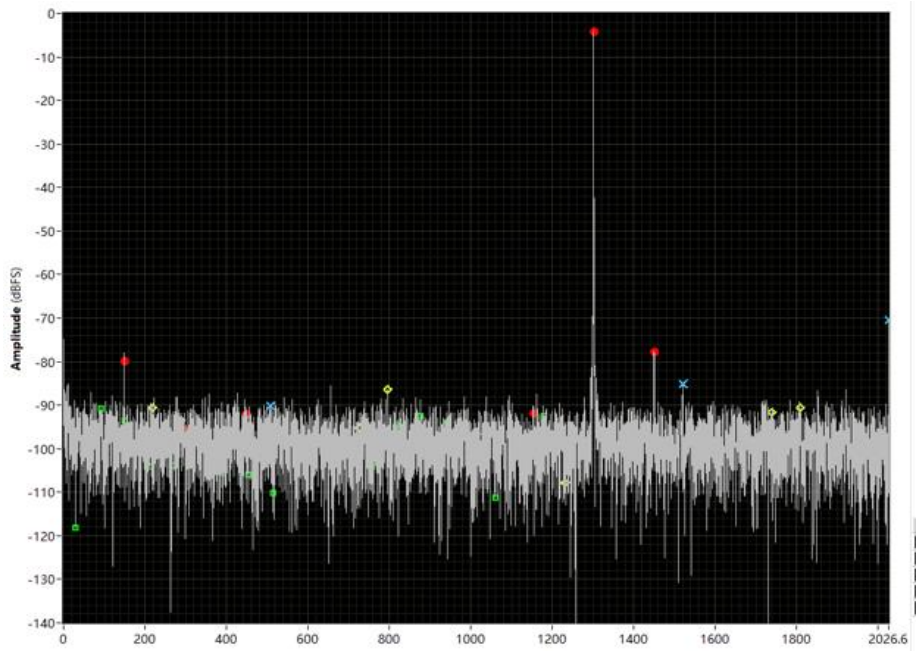
RFSoC PCIe的功能框图

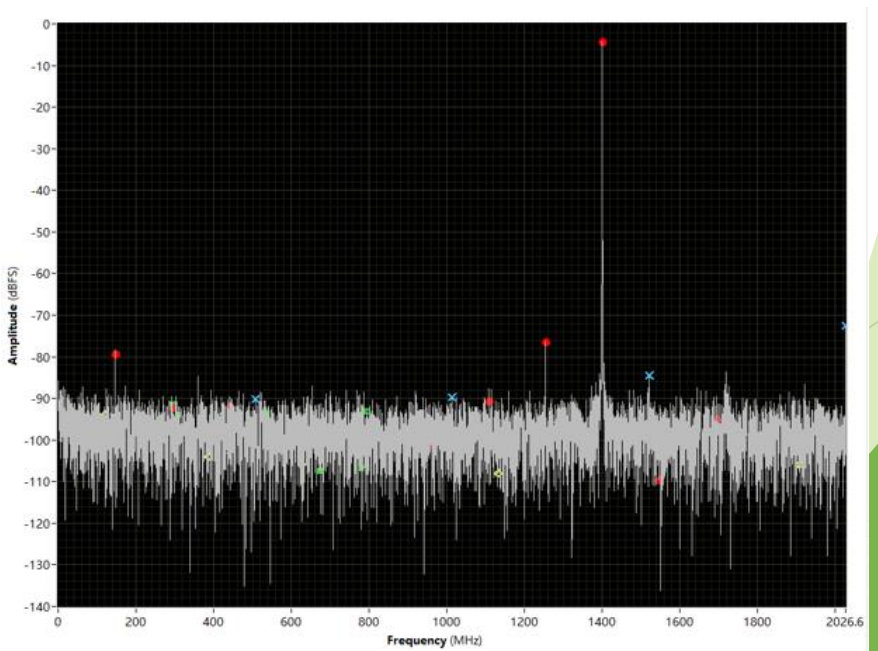


前面板	■	8x ADC， SSMC接口
	■	1x Trig， SSMC接口
	■	1x CLK， SSMC接口
板上资源	■	Xilinx RFSoC 三代 FPGA
	■	8GB DDR4 连接至PL
	■	4GB DDR4 连接至PS
	■	GbE连接至PS
接口	PCIe Gen3 x16至HostPC	

ADC性能指标（参考）

采样信号	信号功率（dBFS）	SFDR（dBc）	SFDRxH23（dBc）	SNR（dBFS）
1300MHz	-4.04	71.95	71.95	52.98
1400MHz	-4.25	72.04	73.99	52.58





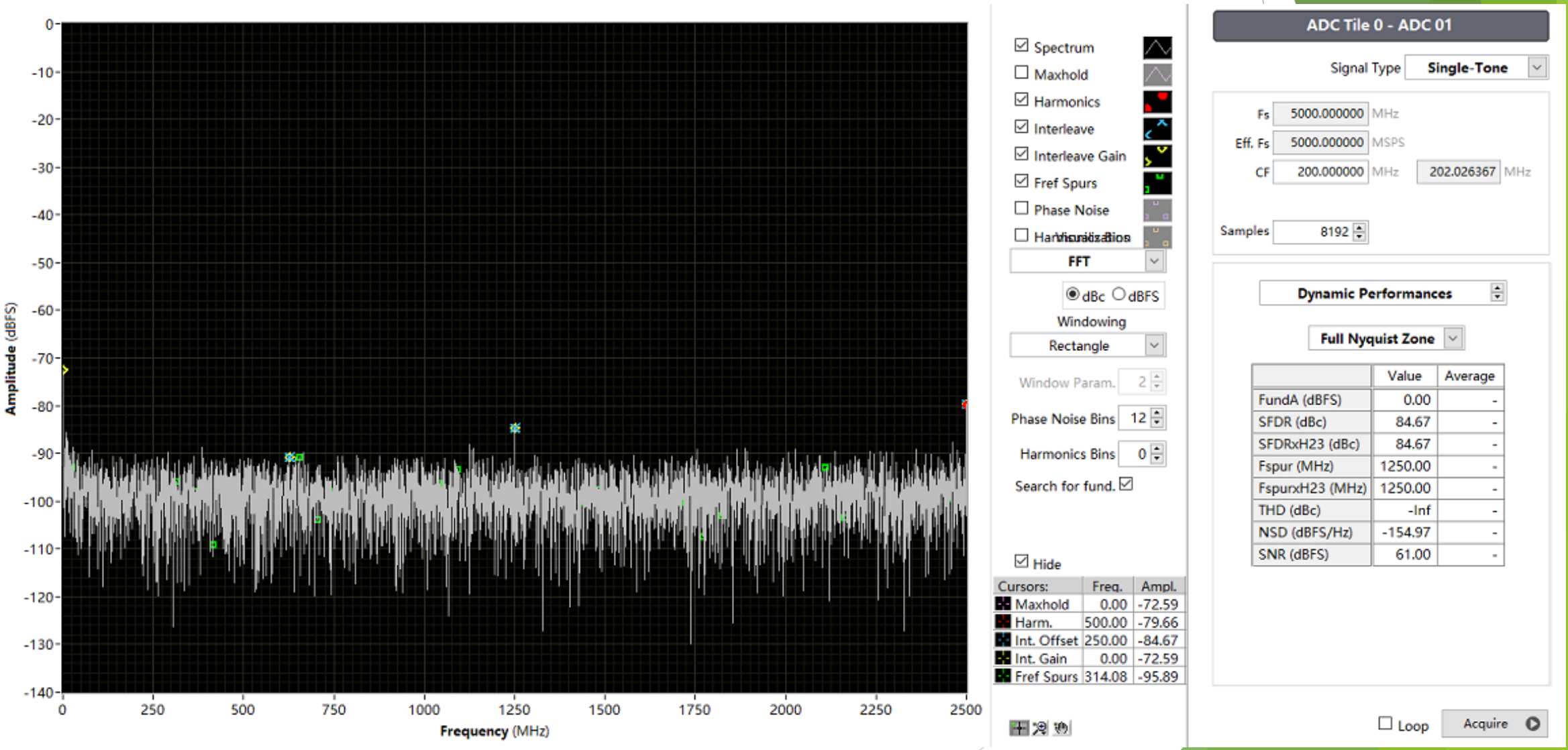
通道隔离度

信号频率：2.4Ghz	信号 ON	信号 OFF	粗略计算
Bank 225，通道 0	-8.9	-88	
Bank 225，通道 1	-74.1	-91	65.2dB
Bank 224，通道 1	-82	-91	73.1dB

信号频率：1.6Ghz	信号 ON	信号 OFF	粗略计算
Bank 225，通道 0	-7.13	-88	
Bank 225，通道 1	-81	-90	73.87dB
Bank 224，通道 1	-84	-90	76.87dB

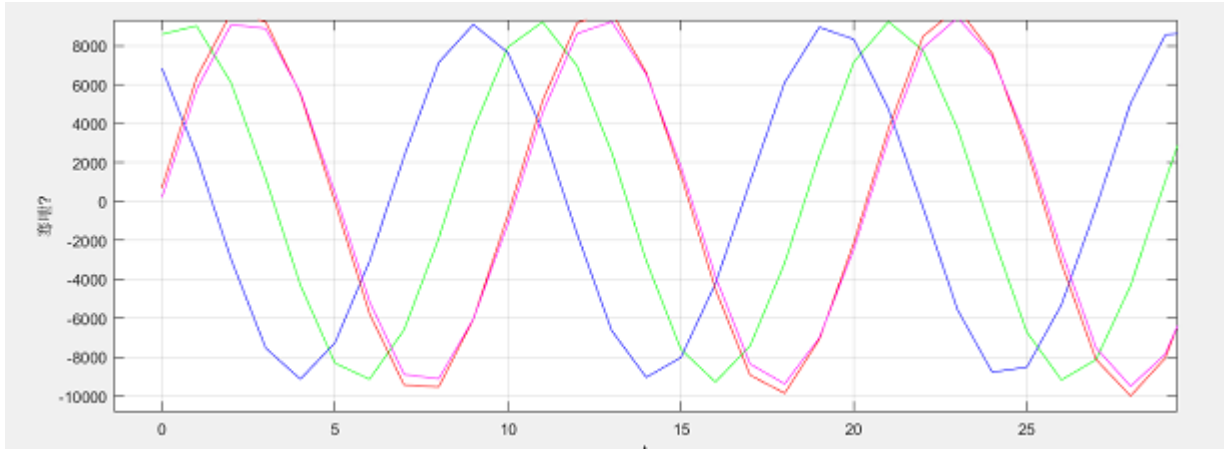
信号频率：400Mhz	信号 ON	信号 OFF	粗略计算
Bank 225，通道 0	-8	-90	
Bank 225，通道 1	-90	-90	82dB
Bank 224，通道 1	-90	-90	82dB

底部噪声

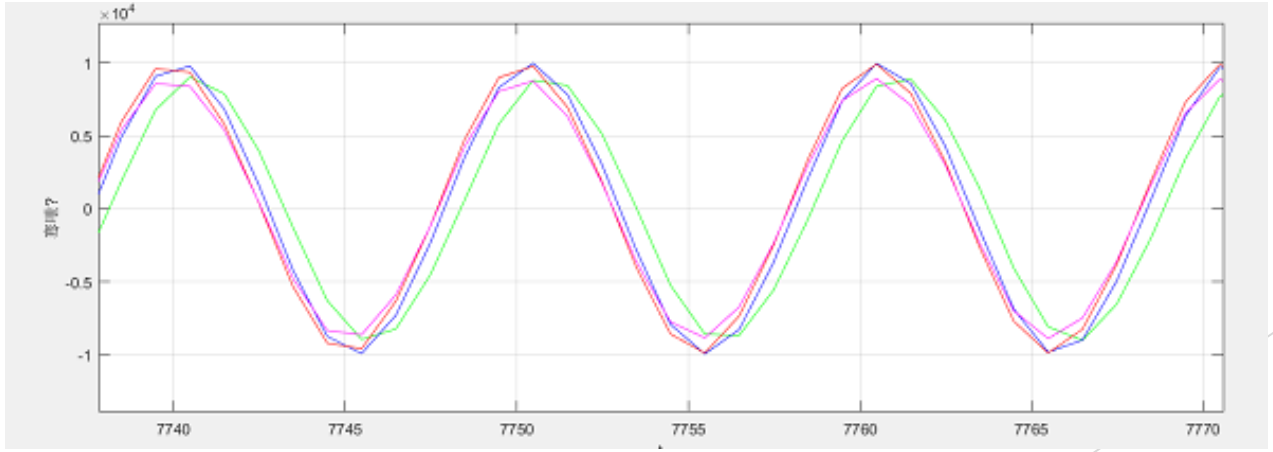

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
Amplitude (dBFS)
0
250
500
750
1000
1250
1500
1750
2000
2250
2500
Frequency (MHz)
Spectrum
Maxhold
Harmonics
Interleave
Interleave Gain
Fref Spurs
Phase Noise
FFT
dBc
dBFS
Windowing
Rectangle
Window Param. 2
Phase Noise Bins 12
Harmonics Bins 0
Search for fund.
Hide
Cursors: Freq. Ampl.
Maxhold 0.00 -72.59
Harm. 500.00 -79.66
Int. Offset 250.00 -84.67
Int. Gain 0.00 -72.59
Fref Spurs 314.08 -95.89
ADC Tile 0 - ADC 01
Signal Type Single-Tone
Fs 5000.000000 MHz
Eff. Fs 5000.000000 MSPS
CF 200.000000 MHz 202.026367 MHz
Samples 8192
Dynamic Performances
Full Nyquist Zone
Value Average
FundA (dBFS) 0.00 -
SFDR (dBc) 84.67 -
SFDRxH23 (dBc) 84.67 -
Fspur (MHz) 1250.00 -
FspurxH23 (MHz) 1250.00 -
THD (dBc) -Inf -
NSD (dBFS/Hz) -154.97 -
SNR (dBFS) 61.00 -
Loop
Acquire

通道一致性

一般板卡



RISN-5088

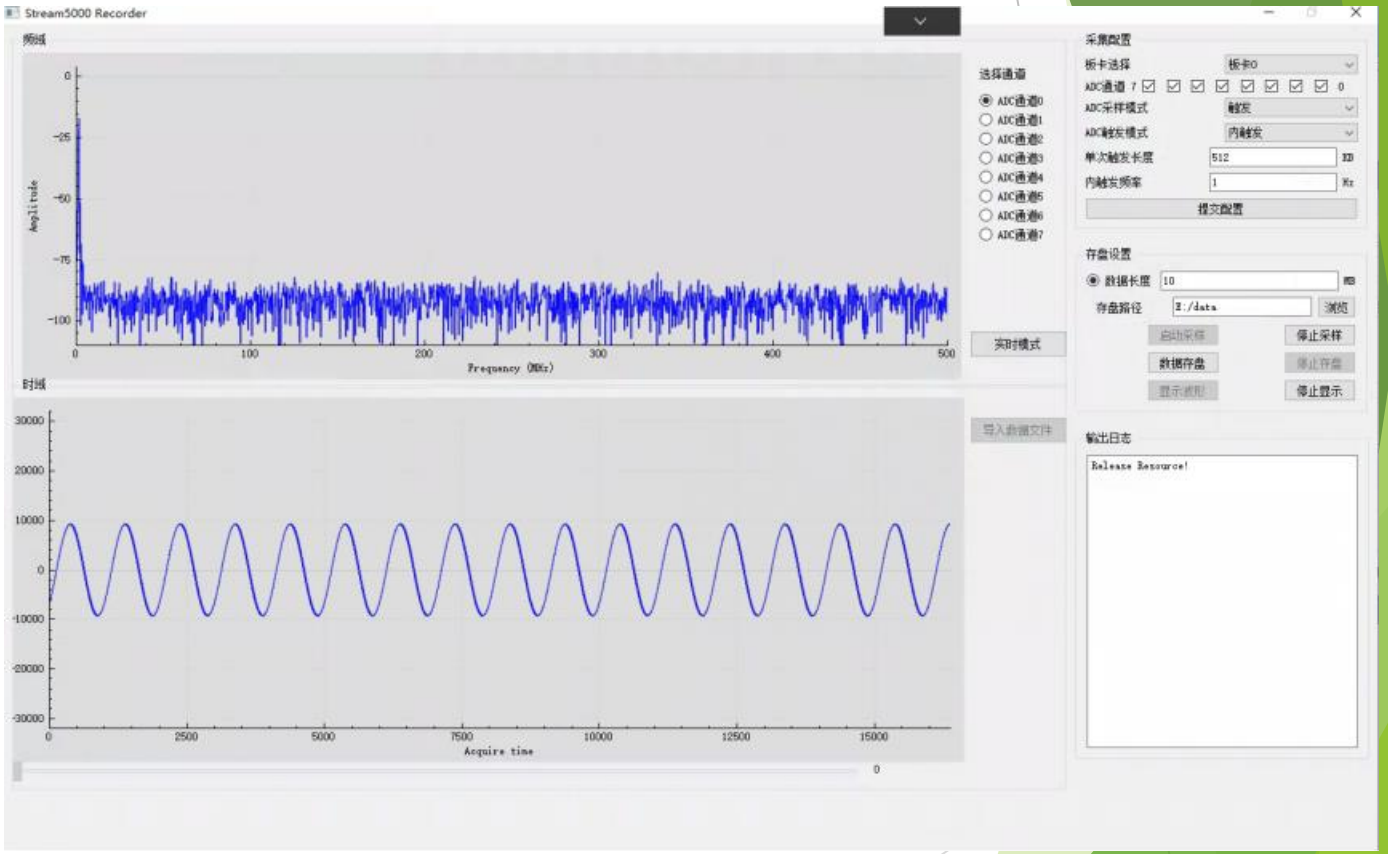


上位机软件

- 设置工作参数
- 时域显示
- 频域显示

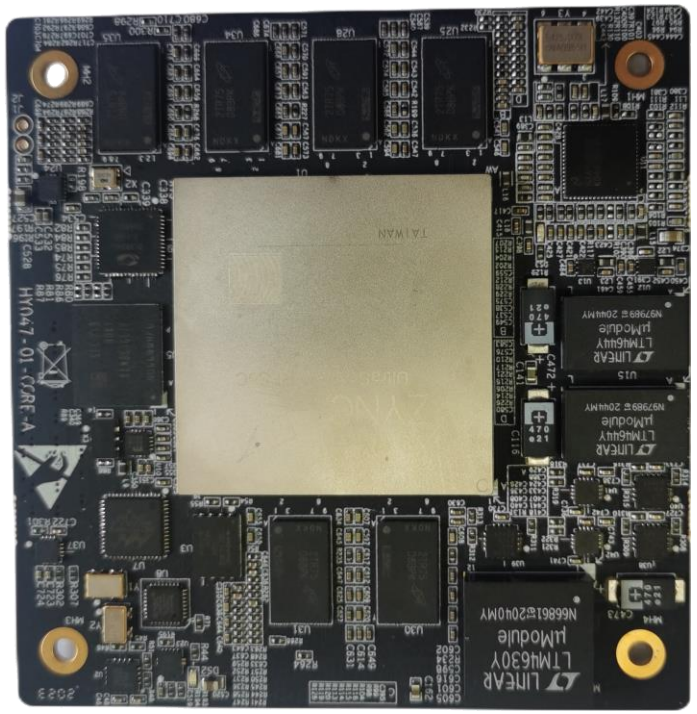
✓ Windows
✓ Linux

可向客户提供操作软件的源码，协助客户快速应用开发！

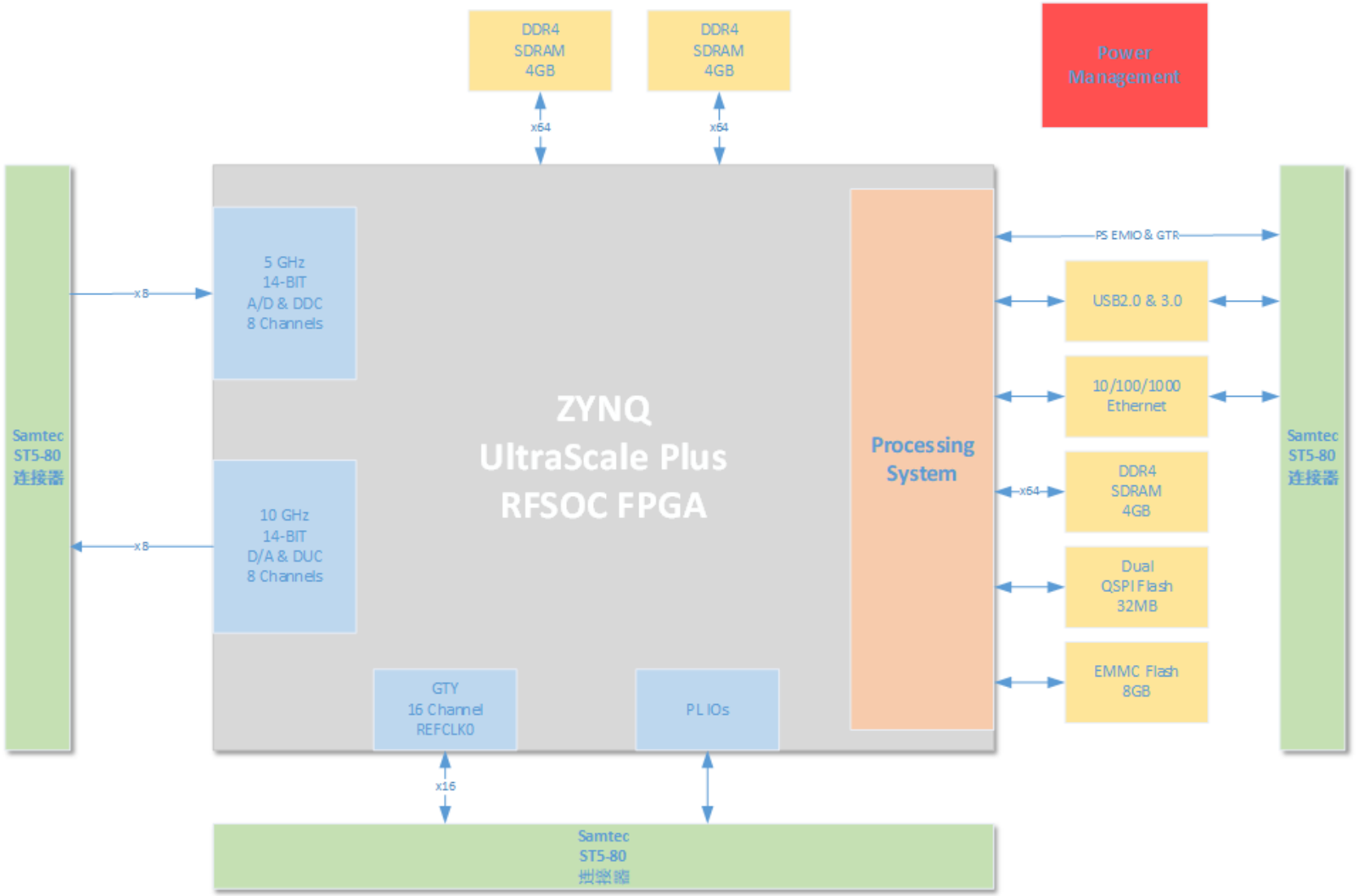


RFSoC 核心板——快速定制的利器！！

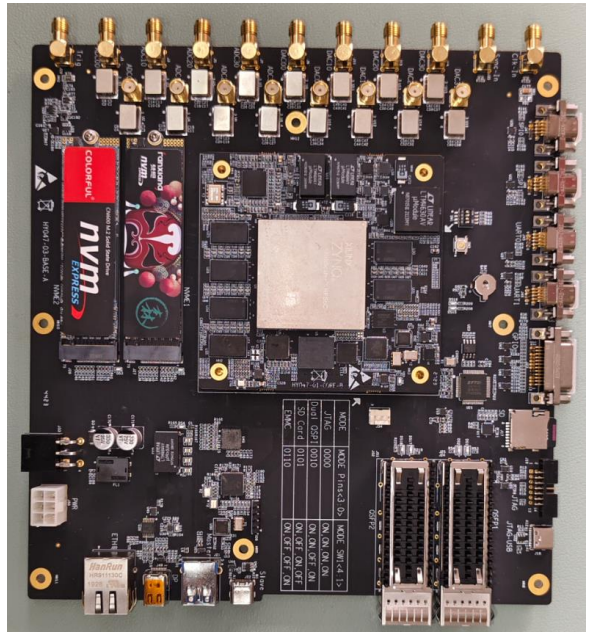
- 基于Zynq RFSoC三代 FPGA
- 8路最高5G SPS ADC
- 8路最高10G SPS的DAC
- 90 x 90 mm
- PCIe Gen3 x16，高速数据通讯
- PL部分8GB DDR4
- PS部分4GB DDR4
- 支持外部时钟输入



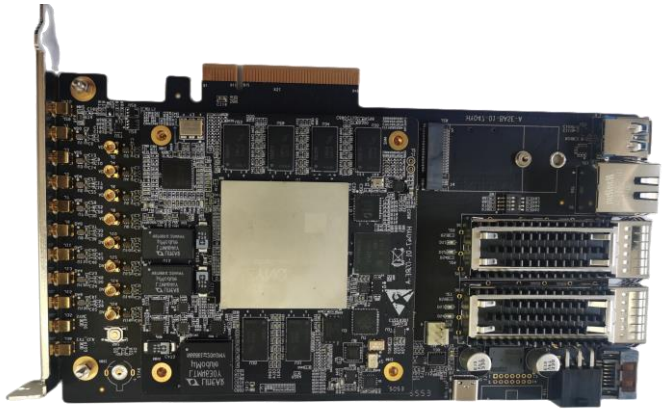
RFSoC 核心板功能框图



RFSoC 核心板的载板

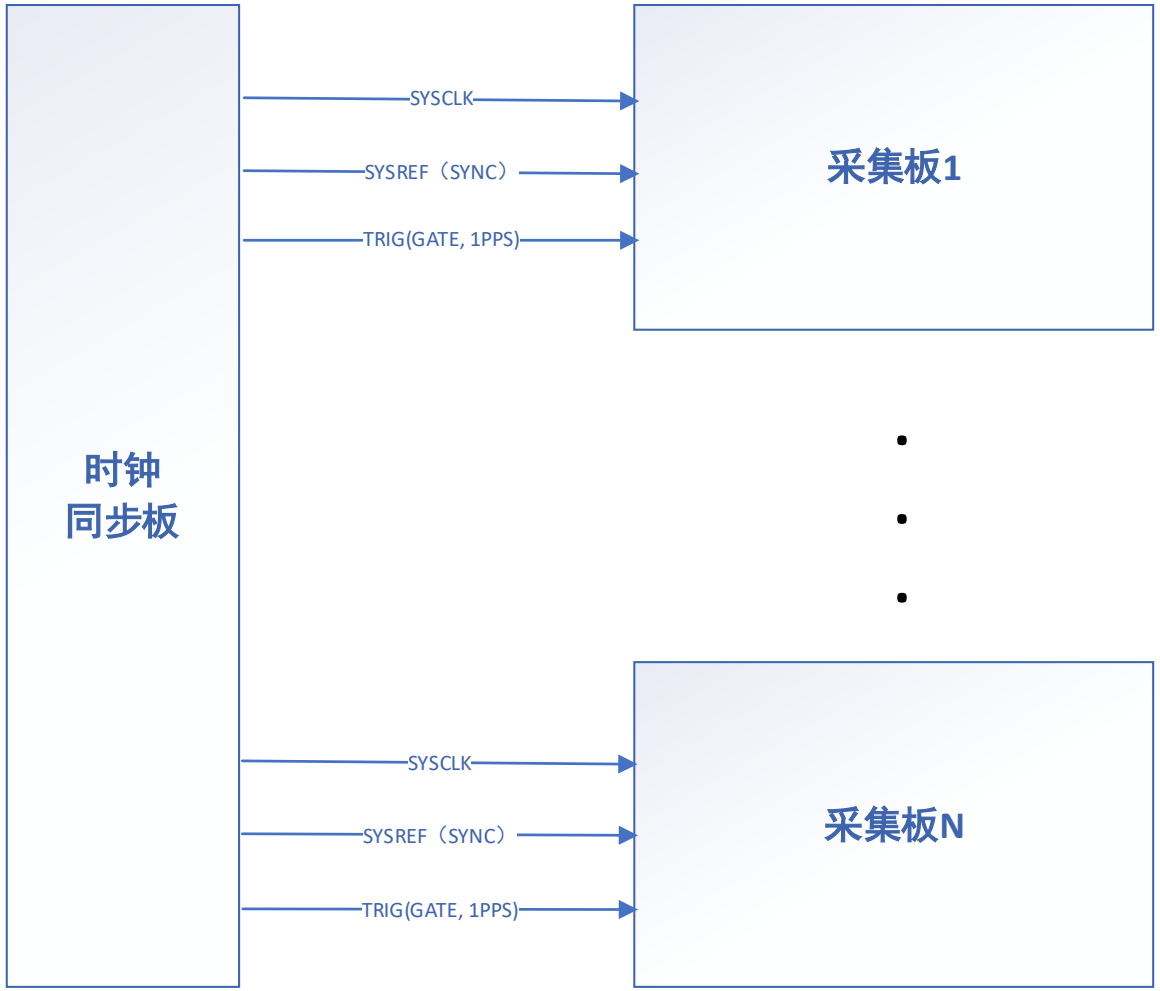


独立载卡



PCIe载卡

板间时钟同步



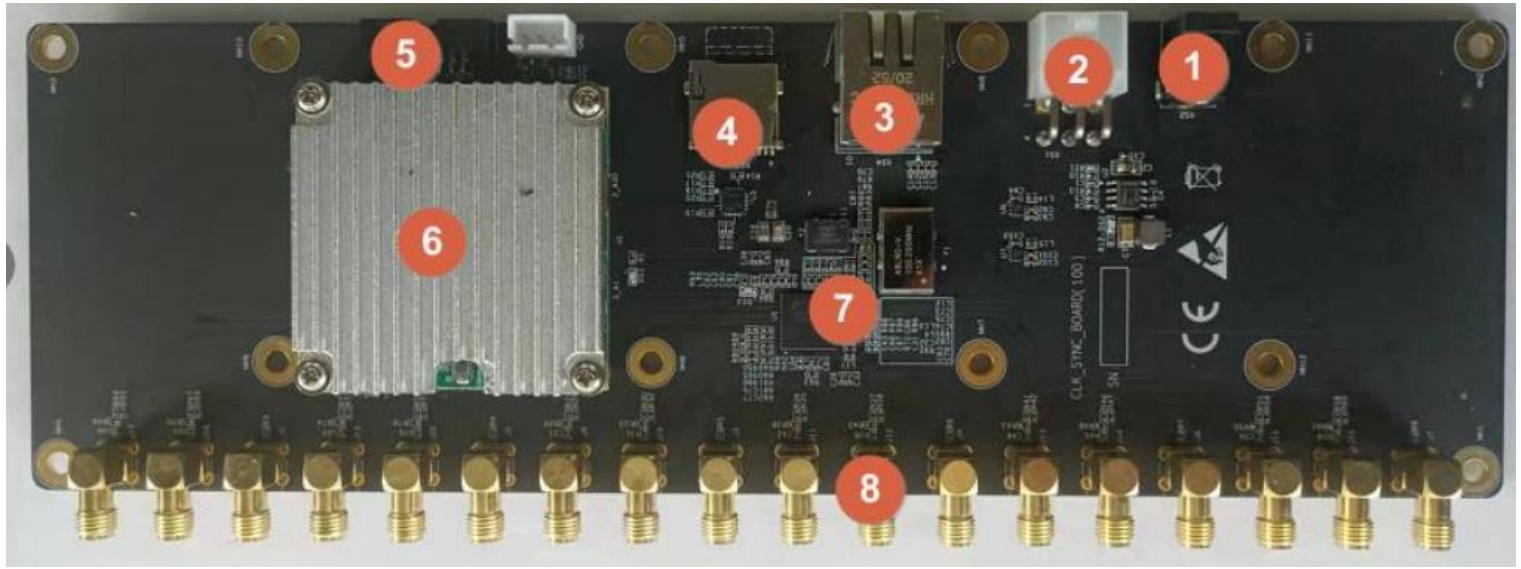
板间同步的关键

所有的板卡使用同源的
- FPGA SYSREF
- 采样时钟
- 触发信号

对相差进行补偿
- FPGA软件补偿 SIN（x + θ）
- 同步卡对采样时钟等信号进行相移
- 调整线缆长度等物理方法

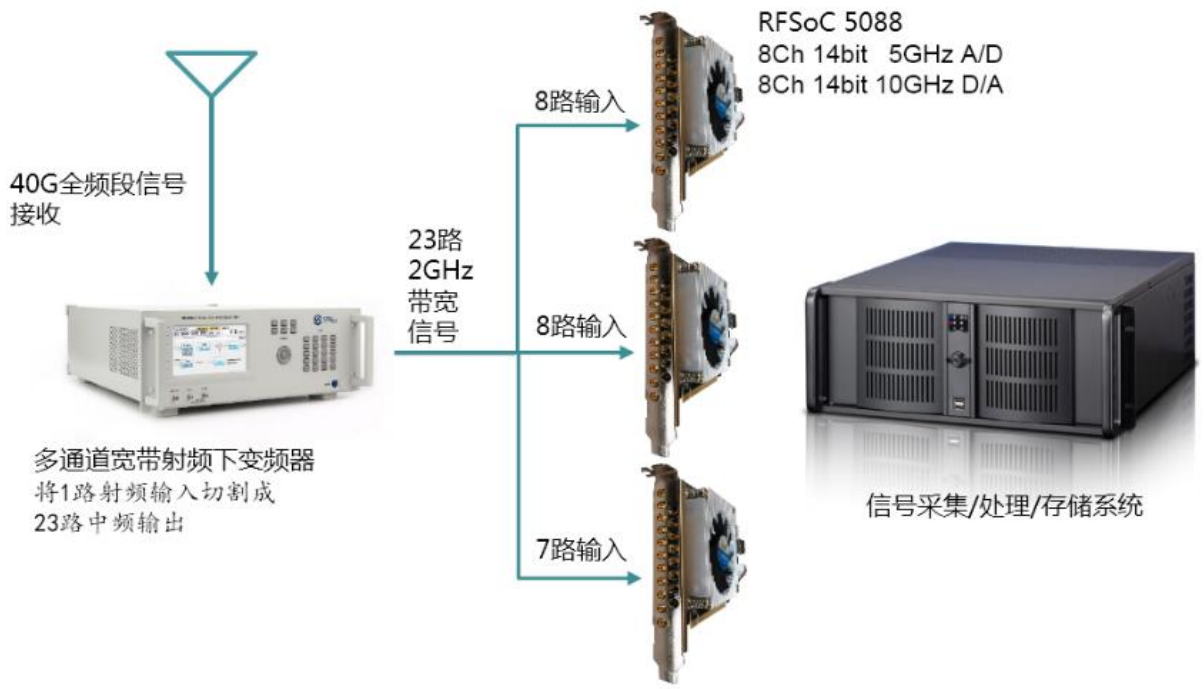
工作在稳定的环境中
- 温度恒定
- 避免振动、重插线缆等物理影响

板间同步卡



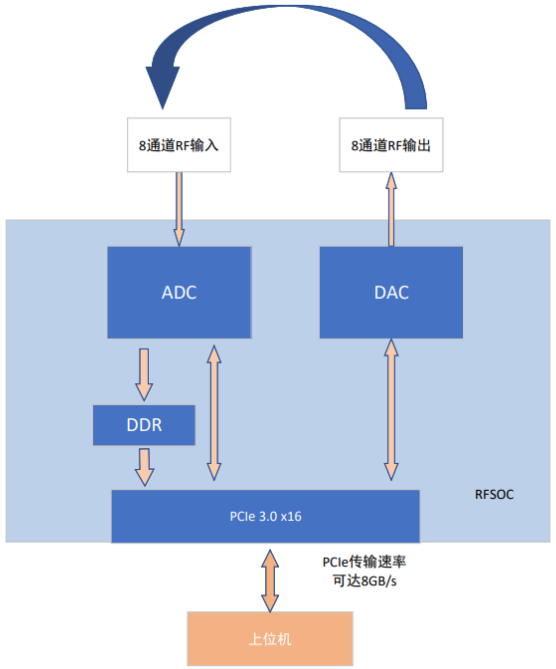
部件序号	功能描述
1	圆形电源输入口，12V@1A
2	ATX 形式电源输入口，12V@1A
3	千兆网口
4	TF 卡接口
5	标准 Xilinx 2x7 mm JTAG 接口
6	Zynq 主控模块，采用的米联客 MZ7XA 模块
7	时钟部分，包括 LMK04828，以及 VCXO，TCXO
8	SMA 输出，一共有 6 组，每组包括 1 个 CLK，1 个 TRIG，一个 SYNC

应用案例1- 40GHz宽带扫频



- ✓ 1台超宽带多通道射频下变频器，可以接收40GHz带宽的信号
- ✓ 频域切割成23路带宽为2GHz的中频信号同步输出
- ✓ 3块RFSoC 5088模块，提供24路5GHz采样率的同步采集；

应用案例2-空域信号环境分析平台



- ✓ 8通道DAC循环播放数据文件，输出RF信号至天线
- ✓ 8通道ADC从天线端接收反射回来的RF信号
- ✓ 对比分析收发数据，进行空域信号环境分析